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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,419	11/12/2003	Paul D. Stultz	016295.1471	6796

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,419	STULTZ, PAUL D.	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodman et al (US6282601) hereinafter Goodman in view of Sedmak (US20040019722).

4. As to claim 1, Goodman discloses an information handling system, comprising: a plurality of processors coupled to a processor bus (Goodman teaches in figure 1 of a plurality of processors 12a, 12b ... 12n, COL. 3, lines 1 - 10)., and
a memory (a system memory 16 in figure 1, COL. 3, lines 1 - 10).,

Goodman does not explicitly teach wherein each of the processors is operable to enteran interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode.

However, Sedmak teaches wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has

exited the interrupt mode. Sedmak teaches in figure I of a multiple processor system with processors 104(1) and 104(2), comprising unique semaphore request and grant bits (106(1) and 106(2)). This system is coupled to a semaphore arbiter CAU, 110, which determines which processor has access to the shared resource 105.
It would have been obvious to one of ordinary skill in the art at the time of the invention to use the semaphore system of Sedmak in the computer system of Goodman to have a means of managing the interrupts in a multi-processor system, page 1, paragraph 0010. One of ordinary skill in the art would have been motivated to use the semaphore system of Sedmak in the computer system of Goodman to have a means of managing the interrupts in a multi-processor system, page 1, paragraph 0010);
each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (the semaphores are stored in control register 106(1) and 106(2) , page 1, paragraph 0016).

5. As to claim 2, Sedmak discloses the information handling system, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016).

6. As to claim 3, Sedmak discloses the information handling system, wherein each processor is operable to access the semaphores associated with the processors

of the information handling system (Each processor has said access via the CAU unit. That arbitrates all semaphore requests, page 1, and paragraph 0016).

7. As to claim 4, Sedmak discloses wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis (Each processor has said access via the CAU unit. That arbitrates all semaphore requests, page 1, and paragraph 0016).

8. As to claim 5, Goodman discloses the information handling system, wherein the memory location associated with the storage of the semaphores associated with the processors of the information handling system is memory space dedicated to storing data associated with the entry of the processors into interrupt mode (Said memory space allocation for interrupt sequences, such as power-on self test, COL. 4, lines 10 – 18).

9. As to claim 6, Goodman discloses the information handling system, wherein the the interrupt mode is system management interrupt mode (said mode, COL. 3, lines 42 – 45).

10. As to claim 7, Goodman discloses the information handling system, wherein the interrupt mode is a system management interrupt mode (said mode, COL. 3, lines 42 – 45);

Wherein the semaphore associated the semaphore associated with a processor is stored in a memory location that is offset from a base memory location by a unique offset indicator associated with said processor (Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016); and wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis (Each processor has said access via the CAU unit. That arbitrates all semaphore requests, page 1, and paragraph 0016).

11. As to claim 8, Goodman discloses a method for processing an interrupt in a multiple processor computer system, comprising the steps of: for each processor, entering interrupt mode (each processor enters the interrupt mode from the assertion of an SMI interrupt to all processors, COL. 4, lines 54 - 56)., Sedmak teaches for each processor, setting a semaphore associated with the processor to indicate that the processor has exited the interrupt mode, wherein a uniquely addressable semaphore is associated with each processor (Figure 1 illustrates that each processor has a request bit and a grant bit. When the request bit is set to zero, the other processor can be granted access via the arbiter CAU, 110, see figure 2); and teaches for each non-interrupt handling processors, exiting interrupt mode up following the negation of the semaphore associated with the processor (Figure 3 illustrates how the exit phase is accomplished by the processor in step 308, page 3, paragraph 0025).

12. As to claim 9, Sedmak discloses the method for processing an interrupt in a multiple processor computer system, wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis (Figure 3 illustrates said method, page 3, paragraph 0025).

13. As to claim 10, Sedmak discloses the method for processing an interrupt in a multiple processor computer system, wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (Figure 3 illustrates the negation of each semaphore bit in 308 to exit the access phase, page 3, paragraph 0025).

14. As to claim 11, Goodman discloses the method for processing an interrupt in a multiple processor computer system, wherein the interrupt is a system management interrupt (the interrupt mode is said mode, COL. 3, lines 42 - 45).

15. As to claim 12, Sedmak discloses the method for processing an interrupt in a multiple processor computer system, wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique offset indicator (Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016).

As to claim 13, Sedmak discloses the method for processing an interrupt in a

multiple processor computer system, wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis (Figure 3 illustrates said method, page 3, paragraph 0025); wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (Figure 3 illustrates the negation of each semaphore bit in 308 to exit the access phase, page 3, paragraph 0025); and

wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique offset indicator (Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016).

16. As to claim 14, Goodman discloses the method for processing an interrupt in a multiple processor computer system, wherein the interrupt is a system management interrupt (Goodman teaches of the interrupt mode is said mode, COL. 3, lines 42 - 45),

Sedmak teaches wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis; wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis

(Figure 3 illustrates the negation of each semaphore bit in 308 to exit the access phase, page 3, paragraph 0025); and

wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016).

17. As to claim 15, Goodman discloses a computer system, comprising'. a plurality of processors, a memory (figure 1 of a plurality of processors 12a, 12b ... 12n, COL. 3, lines 1 - 10);

a memory (a system memory 16 in figure 1, COL. 3, lines 1 - 10),.

wherein the architecture of the processors and the memory is a non-uniform memory access architecture (the support other multiple computer systems comprising numa architecture machines, COL. 2, lines 55 - 67); and

Sedmak teaches wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt Mode (Figure 1 illustrates a multiple processor core 104 comprising a unique addressable semaphore in memory 106, that follows a methodology that informs when the processor has excited the interrupt mode as illustrated in figure 3, step 308, page 3, paragraph 0026).

18. As to claim 16, Goodman discloses the computer system, wherein

the interrupt mode is associated with a system management interrupt (the interrupt mode is said mode, COL. 3, lines 42 - 45).

19. As to claim 17, Sedmak discloses the computer system, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016).

20. As to claim 18, Goodman discloses the computer system, wherein the memory location associated with the storage of the semaphores is memory space dedicated to storing data associated with the entry of the processors into interrupt mode (said memory space allocation for interrupt sequences, such as power-on self test, COL. 4, lines 10 - 18).

21. As to claim 19, Sedmak discloses the computer system, wherein the semaphores may be accessed by each of the processors on a non-exclusive basis (Each processor has said access via the CAU unit. That arbitrates all semaphore requests, page 1, and paragraph 0016).

22. As to claim 20, Sedmak discloses the computer system, wherein the semaphores may be addressed by each of the processors on a non-exclusive basis (Each processor

has said access via the CAU unit. That arbitrates all semaphore requests, page 1, and paragraph 0016); and

wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator ((Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016).

Response to Arguments

23. Applicant's arguments, see a, filed July 3, 2006, with respect to the rejection(s) of claim(s) 1, and 15 under Goodman & Narad have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sedmak.

With respect to claim 1, and 15, the applicant argues that prior art does not teach processors, but computer systems. The examiner points to the teaching of Sedmak as illustrated in figure 1 of a multi-processor device.

With respect to claim 1 and 15, the applicant argues that prior art does not teach uniquely addressable semaphore in memory. The examiner points to the teaching of Sedmak in figure 1 that illustrates unique addressable bits in each processor for semaphore flags.

With respect to claims 1, and 15, the applicant argues that the prior art does not teach a processor exiting the interrupt mode. The examiner points to the teaching of Sedmak in figure 3, step 308 of exiting interrupt mode.

With respect to claim 8, the applicant argues that the prior art does not teach the negation of a semaphore indicating exit from the interrupt mode. The examiner points to the teaching of Sedmak in figure 3, step 308 that offers said teaching.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAD
8/29/2006

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